

Claims

1. A semiconductor integrated circuit device having:
an input terminal for receiving an input signal including any one of an instruction, a data, a position where the data exists, or a timing signal; and

an output terminal for producing a signal formed by the internal circuit in response to the input signal or a signal fed through the input terminal.

2. A semiconductor integrated circuit device according to claim 1, wherein:

the instruction is a command for specifying the state of operation;

the data is the one to be stored;

the position where the data exists is an address signal;

the timing signal is a clock; and

the semiconductor integrated circuit device includes a memory circuit that operates in response to a command and an address signal input in synchronism with the clock.

3. A semiconductor integrated circuit device according to claim 2, wherein the memory circuit replaces the stored data read out according to the address by the input data through the input terminal and produces the input data from the output terminal when it has received a reading operation instruction corresponding to the address assigned thereto.

4. A semiconductor integrated circuit device according

to claim 1, wherein the instruction, the data, the position where the data exists and the timing signal output from the output terminal are those that have been re-adjusted by a timing signal reproduced therein.

5. A semiconductor integrated circuit device according to claim 4, wherein the timing signal that is re-adjusted is the one formed by a phase synchronizing loop circuit that receives a reference timing signal.

6. A semiconductor integrated circuit device according to claim 5, wherein the reference timing signal is the one input from an external unit.

7. A data processing system comprising:

a plurality of semiconductor integrated circuit devices each having an input terminal for receiving an input signal containing any one of an instruction, a data, a position where the data exists or a timing signal, and an output terminal for producing a signal formed in an internal circuit in response to the input signal or fed through the input terminal; and

a signal-forming circuit for forming an input signal containing any one of the instruction, the data, the position where the data exists or the timing signal for the semiconductor integrated circuit devices; wherein

the output terminal of the semiconductor integrated circuit device in the preceding stage and the corresponding input terminal of the semiconductor integrated circuit device

of the next stage are connected in cascade;

the input signal containing any one of the instruction, the data, the position where the data exists or the timing signal formed by the signal-forming circuit is fed to the input terminal of the semiconductor integrated circuit device of the initial stage in the cascade connection; and

among the signals from the output terminal of the semiconductor integrated circuit device of the final stage in the cascade connection, at least the signal corresponding to the data is transmitted to the signal-processing circuit.

8. A data processing system according to claim 7, wherein:

the instruction is a command for specifying the state of operation;

the data is the one to be stored;

the position where the data exists is an address signal;

the timing signal is a clock; and

each of the plurality of semiconductor integrated circuit devices includes a memory circuit that operates in response to a command and an address signal input in synchronism with the clock.

9. A memory system according to claim 8, wherein the command, the data, the address and the timing signal output from the output terminal are those that have been re-adjusted by a timing signal reproduced therein.

10. A memory system comprising a plurality of semiconductor memory devices each having an input terminal for receiving an input signal containing any one of a command, a data, an address or a timing signal, and an output terminal for producing a signal corresponding to the input signal fed through the input terminal, wherein among the plurality of semiconductor memory devices, the output terminal of the semiconductor memory device in the preceding stage and the corresponding input terminal of the semiconductor memory device of the next stage are connected in cascade.

11. A memory system according to claim 10, wherein the input terminal of the semiconductor memory device of the initial stage in cascade receives the command, the data, the address or the timing signal formed by the signal-forming circuit, and, among the output signals produced from the output terminal of the semiconductor memory device in the final stage in cascade, at least a signal corresponding to the data is transmitted to the signal-forming circuit.

12. A memory system according to claim 11, wherein the signal-forming circuit is a memory control device constituted by a semiconductor integrated circuit device.

13. A memory system according to claim 12, wherein the command, the data, the address and the timing signal produced from the output terminal are those that are re-adjusted by a timing signal reproduced therein.

14. A memory system according to claim 13, wherein the timing signal that is re-adjusted is the one formed by a phase synchronizing loop circuit that receives a reference timing signal.

15. A memory system according to claim 12, wherein the data formed by the memory control device are delivered to the input terminals of the plurality of semiconductor memory devices constituting the initial stage, and a plurality of semiconductor memory devices are provided from a next stage up to the final stage being corresponded to the plurality of semiconductor memory devices in the initial stage and are connected in cascade being corresponded thereto in a one-to-one manner.

16. A memory system according to claim 15, wherein the command and the address formed by the signal-forming circuit are transmitted in common to the input terminals of the plurality of semiconductor memory devices constituting the initial stage, and the command and the address are connected in a one-to-one manner being corresponded to the data in the connection of from the output terminals of the plurality of semiconductor memory devices in the initial stage up to the input terminals of the plurality of semiconductor memory devices in the final stage.

17. A memory system according to claim 15, wherein:
the signal-forming circuit forms a plurality of sets of

commands and addresses corresponding to the input terminals of the plurality of semiconductor memory devices constituting the initial stage, and transmits them to the input terminals of the plurality of semiconductor memory devices constituting the initial stage in a one-to-one matter; and

the commands and addresses are connected in a one-to-one manner being corresponded to the data even in the connections of from the output terminals of the plurality of semiconductor memory devices in the initial stage up to the input terminals of the plurality of semiconductor memory devices in the final stage.

18. A memory system according to claim 15, wherein the plurality of semiconductor memory devices replace stored data read out according to the address by the input data through the input terminals and produce the input data from the output terminals when they have received a reading operation instruction corresponding to the addresses assigned thereto.

19. A memory system according to claim 16, wherein the semiconductor memory devices in the preceding stage and the semiconductor memory devices in the succeeding stage to be connected in cascade, are mounted on the front surface and on the back surface of a common mounting board, and are connected in cascade via the through holes.

20. A memory system according to claim 10, wherein the semiconductor memory devices have a buffer circuit for reading,

and include:

a first reading command for reading the stored data from the memory cells and for holding the data in the buffer circuit for reading; and

a second reading command for producing, from the output terminals, the stored data held in the buffer circuit for reading.

21. A memory system according to claim 20, wherein the semiconductor memory devices have a buffer circuit for writing, the write command writes the data fed from the external terminals into the buffer for writing, and the data written into the buffer for writing are autonomously written into the memory cells by the internal control circuit.

22. A memory system according to claim 10, wherein the data are such that among the transmission lines of a number of m , the transmission lines of a number of at least n transit the level periodically.